- - 9. (Newly Added) The system of claim 7, wherein said select transistor and said hold transistor are connected to by a common electrode to at least one of said plurality of data lines. - -

- - 10. (Newly Added) A display system comprising:

an array of pixel cells formed on a substrate, wherein each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate;

a gate (17) line select/hold circuit formed on said substrate and connected to at least one of said plurality of gate lines, a first control pad (25) and a first probe pad (21); and

a data (19) line select/hold circuit formed on said substrate and connected to at least one of said plurality of data lines, a second control pad and a second probe pad, wherein at least one of the gate line select/hold circuit and the data line select/hold circuit comprises first and second transistors each having first and second electrodes defining a serpentine channel region. - -

- - 11. (Newly Added) The system of claim 10, wherein said gate line (17) select/hold circuit is connected to a set of said plurality of gate lines. - -

- - 12. (Newly Added) The system of claim 10, wherein said data line (19) select/hold circuit is connected to a set of said plurality of data lines. - -

- - 13. (Newly Added) The system of claim 10, wherein said gate line select/hold circuit is

connected to a plurality of first control pads. - -

- - 14. (Newly Added) The system of claim 10, wherein said data line select/hold circuit is connected to a plurality of second control pads. - -

- - 15. (Newly Added) The system of claim 10, wherein said gate line select/hold circuit includes a select logic and a hold logic. - -

B2 - - 16. (Newly Added) The system of claim 10, wherein said data line select/hold circuit includes a select logic and a hold logic. - -

- - 17. (Newly Added) The system of claim 10, wherein said gate line select/hold circuit is connected to a third probe pad and third control pad. - -

- - 18. (Newly Added) The system of claim 17, wherein said gate line select/hold circuit comprises:

a select logic connected to said first probe pad and to a plurality of said first control pads; and

(27) (28)

a hold logic connected to said third probe pad and to a plurality of said third control pads.

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(19)

- - 19. (Newly Added) The system of claim 10, wherein said data line select/hold circuit is connected to a third probe pad and third control pad. - -

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- - 20. (Newly Added) The system of claim 19, wherein said data line select/hold circuit comprises:

a select logic connected to said second probe pad and to a plurality of said second control pads; and

a hold logic connected to said third probe pad and to a plurality of said third control pads.

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